

Fundamentals of Computer Engineering

ECE241/340 Laboratory

Lab #4

Sequential circuit design: 2-bit Up/Down Counter

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Honor Pledge:

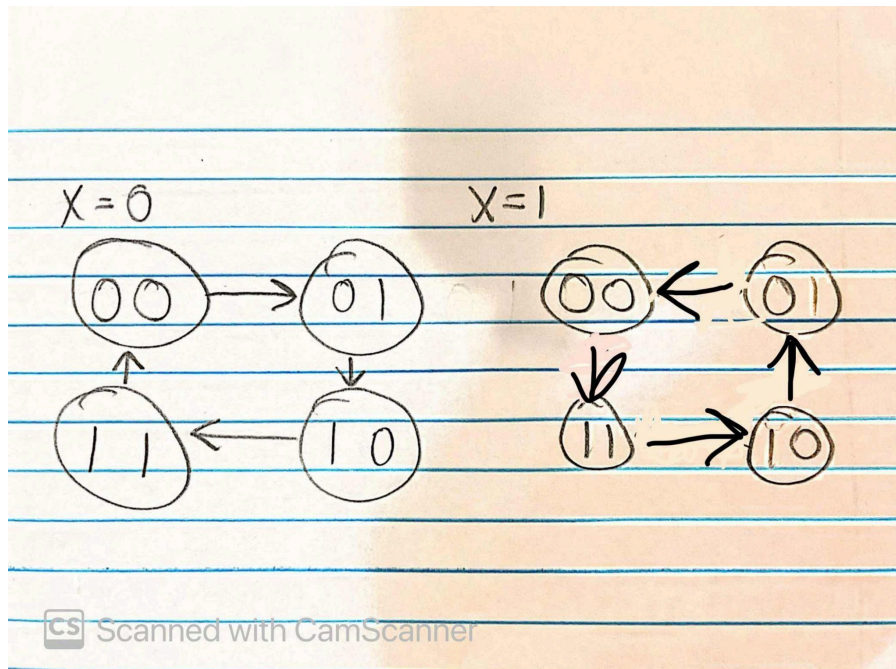
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Introduction

The purpose of this lab is to introduce us to flip-flops, how they work, and how they can be used. In this lab, we are to create a 2-bit up-and-down counter using D flip-flops, a waveform generator, and a short program utilizing the VHDL language. To create the counter I had to use a Moore Finite state machine. A Moore FSM means that the next state only depends on the present state. The objective of the lab is not only to create a counter but a counter that will swap between counting up and down. To make the machine count down, there has to be another input that will make it count backward. The input that is going to be used will be a switch called X. When $X = 0$, the counter will go up as normal, but when $X = 1$ it will start counting backward. We will be able to visually see the flip-flops counting up/down because there will be two LEDs, that will display the state of the machine.

These two state transition tables show what happens to the flow of states depending on the state of X.



This state table shows what the next possible state could be for every state with X as 0 and 1. This table also shows what the LED will display. A 0 will show an unpowered LED and 1 will show a powered LED.

A	B	X	A+	B+
0	0	0	0	1
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	0

I used Kmaps to figure out what the algorithm of each variable is. These variables allow the state to change in the VHDL code.

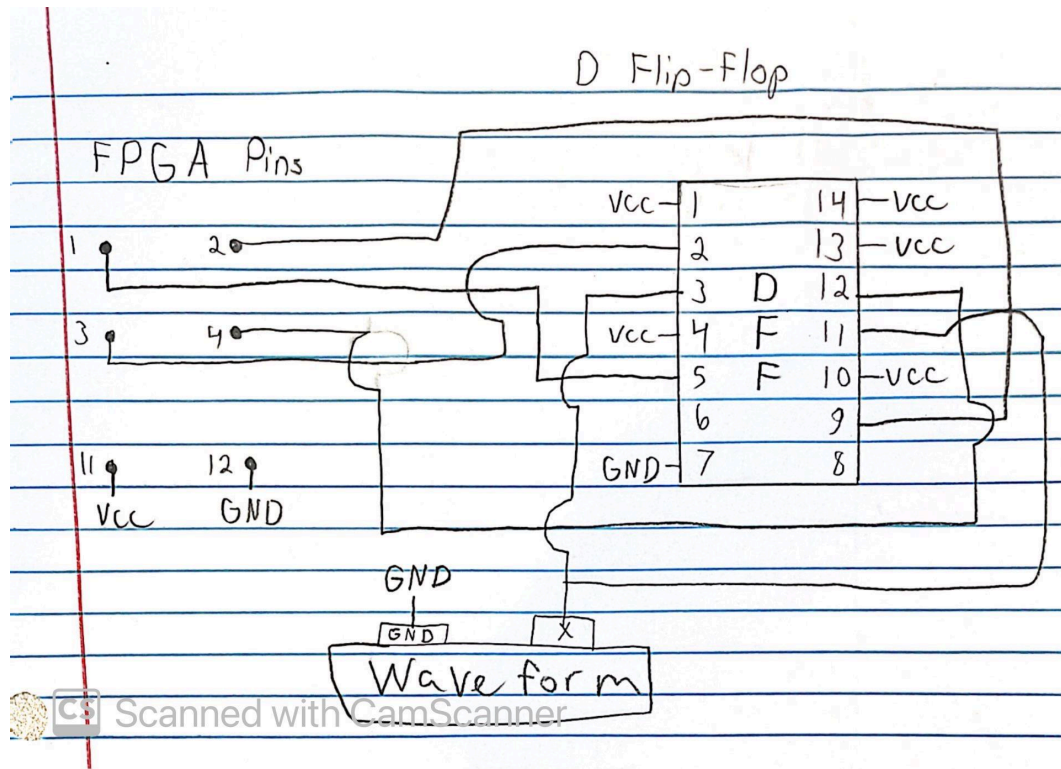
A \ Bx	00	01	11	10
0	0	1	0	1
1	1	0	1	0

A \ Bx	00	01	11	10
0	1	1	0	0
1	1	1	0	0

$A+ = A\bar{B}\bar{X} + \bar{A}B\bar{X} + ABX + \bar{A}B\bar{X}$

$B+ = \bar{B}$

Circuit Diagram



Code

This is the code that I had to write in VHDL using the Quartus compiler.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity Lab4 is
port(
X : in STD_LOGIC;
A : in STD_LOGIC;
B : in STD_LOGIC;
A_next : out STD_LOGIC;
B_next : out STD_LOGIC);
end entity;
architecture arch of Lab4 is
signal x1: std_logic;
Begin
A_next <= A xor (X xor B);
B_next <= not B;

end architecture;
```

Conclusions

Previously I had stated that the objective of this lab was to create an up/down counter using D flip-flops and that I could swap between up and down using the X input of a switch. First had to build the circuit using the circuit diagram above. After creating the circuit, I had to write the VHDL code.

After writing the code I was then able to compile it. I had to then Assign the right pins and then download the output file from the compilation onto the FPGA device. Now all that has to be done is to hook up the waveform generator to the circuit to create the clock pulse. When the clock pulse is on and the FPGA board is programmed, the LEDs will start counting up. The LEDs will start at 00, then go to 01, 10, 11, and then back to 00. If I were to flip the X switch it will then immediately start counting backward instead. For example, if I pressed the switch on 10, it will then go to,01,00, 11, and then back to 10.